

Project
on
Parametric Sensitivity of JLT and Tunnel FET

Submitted in partial fulfillment of the degree of
Master of Science in Electronic Science
Under
Acharya Prafulla Chandra College
West Bengal State University

By

Oindrila Saha
Ishita Das
Soumita Mandal

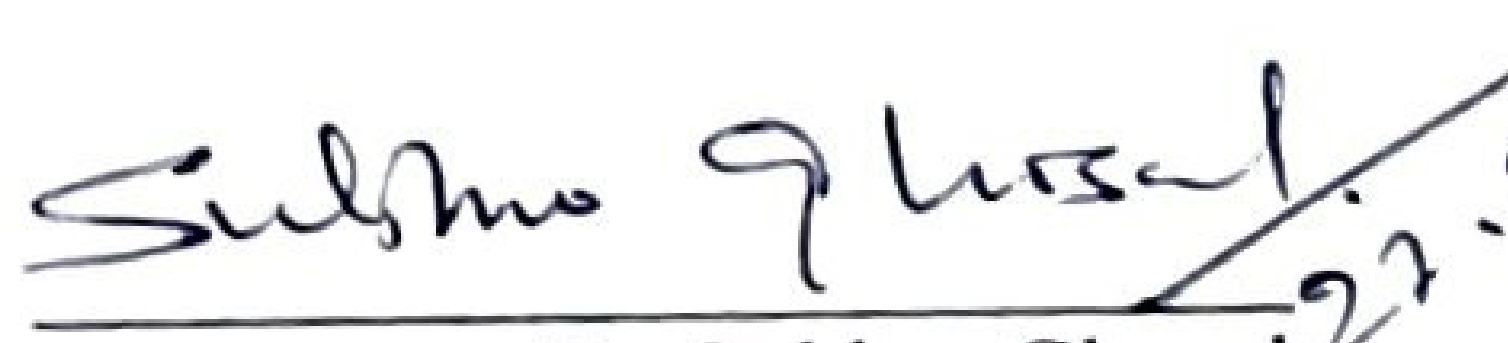
Under the supervision of
Dr. Subhro Ghosal
Department of Electronics
Acharya Prafulla Chandra College

CERTIFICATE

This is to certify that the thesis entitled Design of classical and reversible circuits using a novel QCA based Universal gate *being submitted by----*

- (i) **Oindrila Saha** Roll No. APC/PG(S4)/17/ELTSC/16
Registration No. 1011521400057 of 2015-2016
- (ii) **Ishita Das** Roll No. APC/PG(S4)/17/ELTSC/10
Registration No. 1011521400052 of 2015-2016
- (iii) **Soumita Mandal** Roll No. APC/PG(S4)/17/ELTSC/24
Registration No 1011521400069 of 2015-2016

for the award of the degree of **Master of Science in Electronic Science** is a bona-fide work carried out by him/her under my supervision and guidance. The research reports and the results presented in this thesis have not been submitted in parts or in full to any other University or Institute for the award of any other degree or diploma


Dr. Subhro Ghosal 27.7.17.