Project
on
Parametric Sensitivity of JLT and Tunnel FET

Submitted in partial fulfillment of the degree of
Master of Science in Electronic Science
Under
Acharya Prafulla Chandra College
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By

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CERTIFICATE

This is to certify that the thesis entitled Design of classical and reversible circuits using a novel QCA based Universal gate ***being submitted by----***

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for the award of the degree of **Master of Science** in **Electronic Science** is a bona-fide work carried out by him/her under my supervision and guidance. The research reports and the results presented in this thesis have not been submitted in parts or in full to any other University or Institute for the award of any other degree or diploma

Subhro Ghosal 27.7.17.

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